REMARKS

As noted previously, the Applicant appreciates the Examiner's thorough examination of the subject application.

Claims 1-18 and 21are pending in the application and were rejected in the final Office Action mailed 11 June 2007 on various statutory grounds, as described in further detail below.

Applicant requests reconsideration and further examination of the subject application in light of the following remarks.

Claim Rejections – 35 U.S.C. § 102

Concerning items 1-12 of the Office Action, claims 1-2, 5-7, 11, 14-16, 18, and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,922,065) to Hull et al. ("Hull"). Applicant respectfully traverses the rejection and requests reconsideration for the following reasons.

For a rejection under 35 U.S.C. § 102(b) to be proper, the cited reference must teach, either expressly or inherently, each and every limitation of the claim(s) at issue. In this situation, Hull fails to teach (or suggest) each and every limitation as arranged in claims1-2, 5-7, 11, 14-16, 18, and 21. Applicant therefore submits that the rejection is improper and should be withdrawn accordingly.

For the rejection, the Examiner states that Hull discloses "... *a control processing channel ... including a control register file having a first bit width* (the Examiner considers the branch register file 17 of Hull to be a control register file)*; and a data processing channel ... including a data register file having a second bit width wider than the first bit widths ...*" (the Examiner considers the general purpose register file 12 of Hull to be a data register file).

The Examiner further states that the data registers are 128 bits and the branch registers are 64 bits and therefore Hull discloses a "*control register file having a first bit width; and ... a data register file having a second bit width wider than the first bit widths*".

The Hull reference itself, however, explicitly discloses at column 3, lines 1 to 30, a general purpose register file 12 comprising a set of 128 (**64 bit**) registers [i.e. there are 128 general registers each having a bit width of 64 bits], and a branch register file 17 comprising a set of 8 (**64 bit**) registers [i.e. there are 8 branch registers each having a bit width of 64 bits]. Therefore, it is clear from the teachings of Hull that the general purpose register file 12 of Hull (which the Examiner considers to be a control register file), and the branch register file 17 of Hull (which the Examiner considers to be a data register file) have the same bit width.

Consequently, Hull does not disclose "... *a control processing channel ... including a control register file having a first bit width; and a data processing channel ... including a data register file* ***having a second bit width wider than the first bit widths*** ..."

Furthermore, Hull discloses, at column 3 lines 61 to 63, that "*all instructions in the instruction set of the processor are 41 bits in length*" [i.e. all the instructions have the same bit width].

In addition, Hull does not disclose "*a data processing channel capable of performing data processing operations* ***at least one input of which is a vector***, ...". Hull does not disclose vectors.

Therefore, Applicant respectfully disagree with the Examiner's contention that Hull discloses all the features of claim 1. Hull does not disclose, at least, "*a control processing channel ... including a control register file having a first bit width; and a data processing channel capable of performing data processing operations* ***at least one input of which is a vector***, *the data processing channel ... including a data register file* ***having a second bit width wider than the first bit widths***".

Consequently, independent claims 1 and 18, and their dependent claims, are novel over Hull.

With reference to independent claim 21, Hull does not disclose instruction packets including "*at least one* ***indicator bit*** *at a designated bit location within the instruction packet, wherein ... said indication bit is adapted to cooperate with a decode unit of the computer* ***to designate whether: a) the instruction packet defines a plurality of only control instructions or a plurality of instructions comprising at least one data processing instruction; and b) in the case when there is a plurality of instructions comprising at least one data instruction, the nature of each of the first and second instructions selected from: a control instruction; a data instruction; and a memory access instruction***".

Hull disclose at column 3, line 65 to column 4, line 1 that "*the template field specifies the mapping of instruction slots to execution unit types. The template filed also specifies instruction group boundaries within a bundle*". Hull does not disclose an indicator bit indicating whether the instructions packet comprises a plurality of only control instructions or a plurality of instructions comprising at least one data processing instruction.

Consequently, independent claim 21 is novel over Hull.

Thus, for at least the foregoing reasons, Hull fails to teach (or suggest) all of the limitations of independent claims 1, 18, and 21 of the subject application. Hull therefore forms an improper basis for a rejection of claims 1-2, 5-7, 11, 14-16, 18, and 21 under 35 U.S.C. § 102(b), and Applicant requests that the rejection of these claims be removed accordingly.

Claim Rejections – 35 U.S.C. § 103

Claims 3, 4, and 17

Concerning items 13-17 of the Office Action, claims 3, 4, and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hull, cited previously, in view of "Unifying FPGAs and SIMD Arrays" by Bolotski et al. ("Bolotski"). Applicant traverses the rejection and requests reconsideration for the following reasons.

One requirement for a claim rejection under 35 U.S.C. § 103(a) is that the cited reference(s) teach or suggest each and every limitation as recited in the claim(s) at issue. Another requirements for a rejection under 35 U.S.C. § 103(a) is that proper motivation exist to combine or modify the teachings of the reference(s) in the way proposed by the Examiner for the rejection. As will be explained, one or both of these requirements are not met for the current situation, and the claim rejection is therefore improper.

As stated at page 5, lines 17 to 23 of the application as filed "*The data widths, operators, and other characteristics of the two execution paths 102, 103 differ according to the different characteristics of control code and datapath code. Typically, control code favours fewer, narrower registers, is difficult to parallelize, is typically (but not exclusively) written in C code or another high-level language, and its code density is generally more important than its speed performance. By contrast, datapath code typically favours a large file of wide registers, is highly parallelizable, is written in assembly language, and its performance is more important than its code density*". Consequently, the provision of separate control and data processing paths, takes advantage of the different characteristics of the control and data code. The control code has a narrower bit width and is processed in serial, whereas the data code has a wider bit width and is processed quickly using parallel or serial processing.

Hull does not disclose the use of different bit widths for control and data code, and does not teach how to process control and data code which has different bit widths. Hull explicitly states that the instructions have the same width (41 bits) and aims to execute two instructions (control or data) in parallel. Thus, Hull teaches away from the claimed invention. Additionally, Hull does not teach optimizing the processor in accordance with the different characteristics of control and data code. Furthermore Hull does not disclose vector operations.

The Examiner cites Bolotski as teaching a system than can simulate SIMD and configurable operations on the same and for teaching that the advantages of combining a SIMD and a configurable unit include reducing costs. Bolotski is not understood as teaching the deficiencies noted previously

for Hull relative to independent claim 1 of the subject application (the base claim for claims 3, 4, and 17).

Consequently, when provided with Hull (and/or Bolotski), it would not have been obvious to a person skilled in the art how to amend the processor of Hull such that the processor of the claimed invention results. Thus, claim 1 and its dependent claims are patentable (e.g., not obvious) over the teachings of Hull and/or Bolotski. Accordingly, Hull and Bolotski (whether considered alone or in combination) fails to teach or suggest each and every limitation of independent claim 1 of the subject application. For at least the foregoing reasons, the cited combination of Hull and Bolotski forms an improper basis for a rejection of claims 3, 4, and 17 under 35 U.S.C. § 103(a), and Applicant requests that the rejection be withdrawn accordingly.

Claims 8-10, 12, and 13

Concerning items 18-19 of the Office Action, claims 8-10, 12, and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hull, cited previously, in view of the holding(s) in In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) and/or In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1076). Applicant traverses the rejection and requests reconsideration as, without acceding to the Examiner's allegations set forth for the rejection, Hull is seen as not teaching or suggesting each and every limitation of claim 1, the base claim for claims 8-10, 12, and 13, as was explained *supra*.

For at least the foregoing reasons, the cited combination of Hull and the holding(s) in In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) and/or In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1076) forms an improper basis for a rejection of claims 8-10, 12, and 13 under 35 U.S.C. § 103(a), and Applicant requests that the rejection be withdrawn accordingly..

Conclusion

In view of the remarks submitted herein, Applicant respectfully submits that all of the pending claims in the subject application are in condition for allowance, and respectfully requests a

Notice of Allowance for the application.

Authorization is hereby given to charge our deposit account, No. 50-1133, for the fees corresponding to a Petition for Extension of Time (one month) under 37 CFR § 1.136, and for any other fees that may be required for the prosecution of the subject application.

If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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